University of Fallujah
College of Information Technology
Department of Cybersecurity

MODULE DESCRIPTION FORM

نموذج وصف المادة الدراسية

Module Information معلومات المادة الدراسية					
Module Title	**Digital Logic Design**			**Module Delivery**	
Module Type	**Core**			☒ **Theory** ☒ **Lecture** ☒ **Lab** ☐ **Tutorial** ☐ **Practical** ☐ **Seminar**	
Module Code	**CYS105**				
ECTS Credits	**5**				
SWL (hr/sem)	**125**				
Module Level	1		**Semester of Delivery**	2	
Administering Department	Dept. of Cybersecurity		**College**	College of Information Technology	
Module Leader	Dr. Omar Salah F. Shareef		**e-mail**	omar.alshareef@uofallujah.edu.iq	
Module Leader's Acad. Title	Asst. Prof.		**Module Leader's Qualification**	Ph.D.	
Module Tutor	Dr. Omar Salah F. Shareef		**e-mail**	omar.alshareef@uofallujah.edu.iq	
Peer Reviewer Name	Dr. Ahmad AlSabhany		**e-mail**	ahmad.alsabhany@uofallujah.edu.iq	
Scientific Committee Approval Date	25-5-2026		**Version Number**	1.0	

Relation with other Modules العلاقة مع المواد الدراسية الأخرى			
Prerequisite module	None	**Semester**	
Co-requisites module	None	**Semester**	

Module Aims, Learning Outcomes and Indicative Contents أهداف المادة الدراسية ونتائج التعلم والمحتويات الإرشادية	
Module Objectives أهداف المادة الدراسية	• Teaching the student the basic concepts of digital logic circuits. • Equipping the student with skills to discuss and solve practical problems related to the topic of digital logic circuits. • The connection between theoretical concepts and practical applications. • Understand Number Systems: Master binary, hexadecimal, and octal number systems, arithmetic operations (addition, subtraction), and error-detecting/correcting codes. • Master Boolean Algebra and Simplification: Utilize Boolean algebra and Karnaugh map techniques to simplify logic functions and minimize circuit complexity. • Design Combinational Circuits: Analyze and design circuits where outputs depend solely on current inputs, such as adders, subtractors, decoders, encoders, and multiplexers. • Design Sequential Circuits: Design and analyze circuits with memory, including latches, flip-flops, and registers. • Apply Logic Gate Technologies: Understand the characteristics of different logic gate families and their practical implementation in digital systems.
Module Learning Outcomes مخرجات التعلم للمادة الدراسية	• Show Understanding of the numbering systems and • conversion between them • Explore various methods for logic function minimization • Describe the differences between sequential and combinational logic circuits. • Differentiate between different logic gates and their functions. • Analyze the combinational and sequential circuits • Design various combinational and sequential circuits • Implement combinational and sequential circuits. • Apply the logic principles to the circuit design. • Use simulation tools to simulate various logic circuits. • Present solutions to some digital circuit designs.
Indicative Contents المحتويات الإرشادية	

Learning and Teaching Strategies استراتيجيات التعلم والتعليم	
Strategies	1. Show Understanding the numbering systems and conversion between them. 2. Define the various methods for logic function minimization. 3. Describe the differences between sequential and combinations logic circuits.

Student Workload (SWL) الحمل الدراسي للطالب محسوب لـ ١٥ اسبوعا			
Structured SWL (h/sem) الحمل الدراسي المنتظم للطالب خلال الفصل	63	**Structured SWL (h/w)** الحمل الدراسي المنتظم للطالب أسبوعيا	4
Unstructured SWL (h/sem) الحمل الدراسي غير المنتظم للطالب خلال الفصل	62	**Unstructured SWL (h/w)** الحمل الدراسي غير المنتظم للطالب أسبوعيا	4
Total SWL (h/sem) الحمل الدراسي الكلي للطالب خلال الفصل	**125**		

Module Evaluation تقييم المادة الدراسية					
		Time/Number	**Weight (Marks)**	**Week Due**	**Relevant Learning Outcome**
Formative assessment	**Assignments**	2	10% (10)	5 and 10	All
	Quiz	1	10% (10)	4	LO #1 - #3
	Quiz	1	10% (10)	9	LO #4 - #6
	Report	1	10% (10)	13	LO #6 - #8
Summative assessment	**Midterm Exam**	2hr	10% (10)	7	LO #1 - #4
	Final Exam	3hr	50% (50)	16	All
Total assessment			100% (100 Marks)		

Delivery Plan (Weekly Syllabus) المنهاج الاسبوعي النظري	
	Material Covered
Week 1	Introduction of Numbering system
Week 2	Number System Operations
Week 3	Binary Arithmetic
Week 4	Logic Gats
Week 5	simplify Boolean logic
Week 6	Boolean logic expression
Week 7	Karnaugh map
Week 8	Midterm
Week 9	Combinational Logic

Week 10	Decoders & Encoders
Week 11	Multiplexers & Demultiplexers
Week 12	Flip-Flop
Week 13	Shift Register
Week 14	Binary Counter
Week 15	Course Revision and Final Review

Delivery Plan (Weekly Lab. Syllabus) **المنهاج الاسبوعي للمختبر**	
	Material Covered
Week 1	Introduction to the laboratory environment. Number system conversions between Decimal, Binary, Octal, and Hexadecimal.
Week 2	Arithmetic operations in different number systems: binary addition, subtraction, multiplication, and division.
Week 3	Binary arithmetic using signed and unsigned numbers, 1's complement and 2's complement representation.
Week 4	Introduction to logic gates. Constructing and testing NOT, AND, OR, NAND, NOR, XOR, and XNOR circuits using simulation software.
Week 5	Verification of Boolean identities and DeMorgan's laws using logic gate circuits.
Week 6	Implementing Boolean expressions using logic gates and verifying outputs through truth tables.
Week 7	Simplification of Boolean expressions using Karnaugh Maps (2-variable, 3-variable, and 4-variable K-Maps).
Week 8	Midterm Practical Examination.
Week 9	Design and simulation of combinational logic circuits from truth tables and Boolean expressions.
Week 10	Design and implementation of Encoders and Decoders using logic gates and simulation software.
Week 11	Design and implementation of Multiplexers and Demultiplexers and their practical applications.
Week 12	Implementation and testing of SR, JK, D, and T Flip-Flops using simulation software.
Week 13	Design and simulation of Shift Registers for serial and parallel data transfer.
Week 14	Design and implementation of asynchronous and synchronous Binary Counters.
Week 15	Integrated digital system design exercise and comprehensive practical review.

Learning and Teaching Resources
مصادر التعلم والتدريس

	Text	Available in the Library?
Required Texts	Digital Electronic, Floyd, Eleventh Edition	Yes
Recommended Texts	Introduction to Logic design, B. Marcovitz, Third Edition	Yes
Websites		

Grading Scheme
مخطط الدرجات

Group	Grade	التقدير	Marks %	Definition
Success Group (50 - 100)	**A** - Excellent	امتياز	90 - 100	Outstanding Performance
	B - Very Good	جيد جدا	80 - 89	Above average with some errors
	C - Good	جيد	70 - 79	Sound work with notable errors
	D - Satisfactory	متوسط	60 - 69	Fair but with major shortcomings
	E - Sufficient	مقبول	50 - 59	Work meets minimum criteria
Fail Group (0 – 49)	**FX** – Fail	راسب (قيد المعالجة)	(45-49)	More work required but credit awarded
	F – Fail	راسب	(0-44)	Considerable amount of work required

Note: Marks Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.