

MODULE DESCRIPTION FORM

نموذج وصف المادة الدراسية

Module Information			
معلومات المادة الدراسية			
Module Title	Logic Design		Module Delivery
Module Type	C		☒ Theory ☐ Lecture ☒ Lab ☒ Tutorial ☐ Practical ☐ Seminar
Module Code	AI106		
ECTS Credits	5		
SWL (hr/sem)	125		
Module Level		Semester of Delivery	
Administering Department	AI	College	Information Technology – University of Fallujah
Module Leader	Assist. Lec. Maryam Hamed Abas Assist. Lec. Marwan Muhammed Alwan		e-mail maryam.h.abass@uofallujah.edu.iq marwan.m.alwan@uofallujah.edu.iq
Module Leader's Acad. Title	Lecturer	Module Leader's Qualification	Msc.
Module Tutor	Assist. Lec. Maryam Hamed Abas Assist. Lec. Marwan Muhammed Alwan		e-mail maryam.h.abass@uofallujah.edu.iq marwan.m.alwan@uofallujah.edu.iq
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Scientific Committee Approval Date	1/06/2026	Version Number	2.0

Relation with other Modules			
العلاقة مع المواد الدراسية الأخرى			
Prerequisite module	None	Semester	
Co-requisites module	None	Semester	

Module Aims, Learning Outcomes and Indicative Contents أهداف المادة الدراسية ونتائج التعلم والمحتويات الإرشادية	
Module Objectives أهداف المادة الدراسية	• The student should understand number systems and codes and conversion between them. • The student should understand the Boolean expression and how to apply it. • The students should recognize different logic gates and how to use them. • The student should understand how to design a logic circuit. • The students should understand using K-map for simplification.
Module Learning Outcomes مخرجات التعلم للمادة الدراسية	- Demonstrate a solid understanding of digital logic principles, including Boolean algebra, logic gates, truth tables, and the concept of binary representation.
Indicative Contents المحتويات الإرشادية	- Introduction to Digital Logic - Combinational Logic Design - Arithmetic circuits - Sequential Logic Design - Circuit Testing and Verification.

Learning and Teaching Strategies استراتيجيات التعلم والتعليم	
Strategies	- Conceptual Understanding - Problem-Solving Approach - Hands-on Laboratory Experience - Design Projects - Simulation and Modeling - Problem-Based Learning

Student Workload (SWL)			
الحمل الدراسي للطالب محسوب لـ ١٥ اسبوعا			
Structured SWL (h/sem) الحمل الدراسي المنتظم للطالب خلال الفصل	78	Structured SWL (h/w) الحمل الدراسي المنتظم للطالب أسبوعيا	5
Unstructured SWL (h/sem) الحمل الدراسي غير المنتظم للطالب خلال الفصل	47	Unstructured SWL (h/w) الحمل الدراسي غير المنتظم للطالب أسبوعيا	3
Total SWL (h/sem) الحمل الدراسي الكلي للطالب خلال الفصل	125		

Module Evaluation					
تقييم المادة الدراسية					
		Time/Number	Weight (Marks)	Weekly Due	Relevant Learning Outcome
Formative assessment	Quizzes	2	10% (10)	5 and 10	All
	Assignments	2	5% (5)	2 and 12	All
	Projects / Lab.	1	15% (15)	Continuous	All
	Report	2	10% (10)	13	All
Summative assessment	Midterm Exam	2hr	10% (10)	7	All
	Final Exam	3hr	50% (50)	16	All
Total assessment			100% (100 Marks)		

Delivery Plan (Weekly Syllabus)	
المنهاج الاسبوعي النظري	
	Material Covered
Week 1	Introduction: Digital System
Week 2	Number Systems: Octal and Hexadecimal Numbers
Week 3	Number base conversion
Week 4	- Theories of Boolean Algebra - Digital Logic gates
Week 5	Boolean Expression and Truth table
Week 6	- Sum of Product Simplification - Product Of Sum Simplification
Week 7	- Exclusive OR - NAND gates

	● NOR gates
Week 8	Midterm
Week 9	● Two- and Three-Variables Karnaugh Maps. ● Four Variables Karnaugh Maps.
Week 10	Sequential circuits
Week 11	Combinational Logic: Adder “Full, Half”, Subtractor
Week 12	Comparators, Decoders and Encoders
Week 13	Multiplexers (Data Selectors). Demultiplexers
Week 14	Flip-Flops
Week 15	Final Exam

Delivery Plan (Weekly Lab. And Tutorials Syllabus)

المنهاج الاسبوعي للمختبر

	Material Covered
Week 1	Number System
Week 2	Number base conversion 1
Week 3	Number base conversion 2, and Boolean expression
Week 4	Logic gate , AND, OR, NOT, Exclusive, NAND gates & NOR gates
Week 5	Logic gate, Boolean Expression and Truth table
Week 6	Boolean Laws and Circuit Design
Week 7	Sum of Product form and Simplification and Product Of Sum form and Simplification
Week 8	Midterm
Week 9	Minterms / Maxterms, Canonical Form
Week 10	Karnaugh Maps
Week 11	Karnaugh Maps and Sequential circuits
Week 12	Combinational Logic: Adder “Full, Half”, Subtractor Decoders and Encoders
Week 13	Multiplexers (Data Selectors). Demultiplexers
Week 14	Flip-Flops, with applied logic
Week 15	Final

Learning and Teaching Resources

مصادر التعلم والتدريس

	Text	Available in the Library?
Required Texts	Digital Design, 5 th edition by M. Morris Mano	No

Recommended Texts	- <i>Digital Fundamental, 11th edition by Thomas L. Floyd</i>	No
Websites	- https://circuitverse.org/simulator - https://logic.ly/demo/ - https://digisim.io/circuits/new	

Grading Scheme مخطط الدرجات				
Group	Grade	التقدير	Marks %	Definition
Success Group (50 - 100)	A - Excellent	امتياز	90 - 100	Outstanding Performance
	B - Very Good	جيد جدا	80 - 89	Above average with some errors
	C - Good	جيد	70 - 79	Sound work with notable errors
	D - Satisfactory	متوسط	60 - 69	Fair but with major shortcomings
	E - Sufficient	مقبول	50 - 59	Work meets minimum criteria
Fail Group (0 – 49)	FX – Fail	راسب (قيد المعالجة)	(45-49)	More work required, but credit awarded
	F – Fail	راسب	(0-44)	Considerable amount of work required
Note: Marks Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example, a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails," so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.				

Module Contribution:

Mode of Delivery:

Software Used:

Lab Safety and Ethics statement (for university standardization).

- Ethical use of computing resources (e.g., no piracy, respect software licenses).
- Academic integrity (no cheating, plagiarism, proper attribution).
- Data protection (for real datasets).
- Safe usage of lab equipment and network (no illegal downloads, safe browsing).